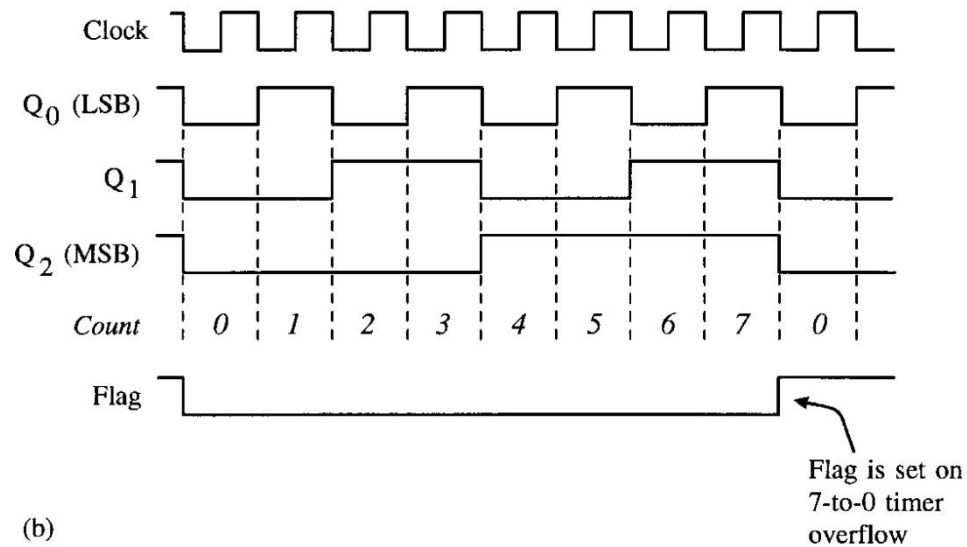
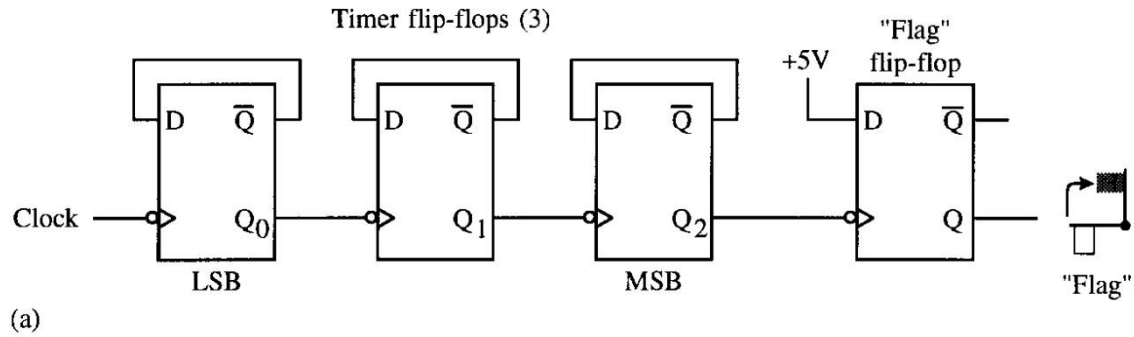

ATmega128

Timer/Counter

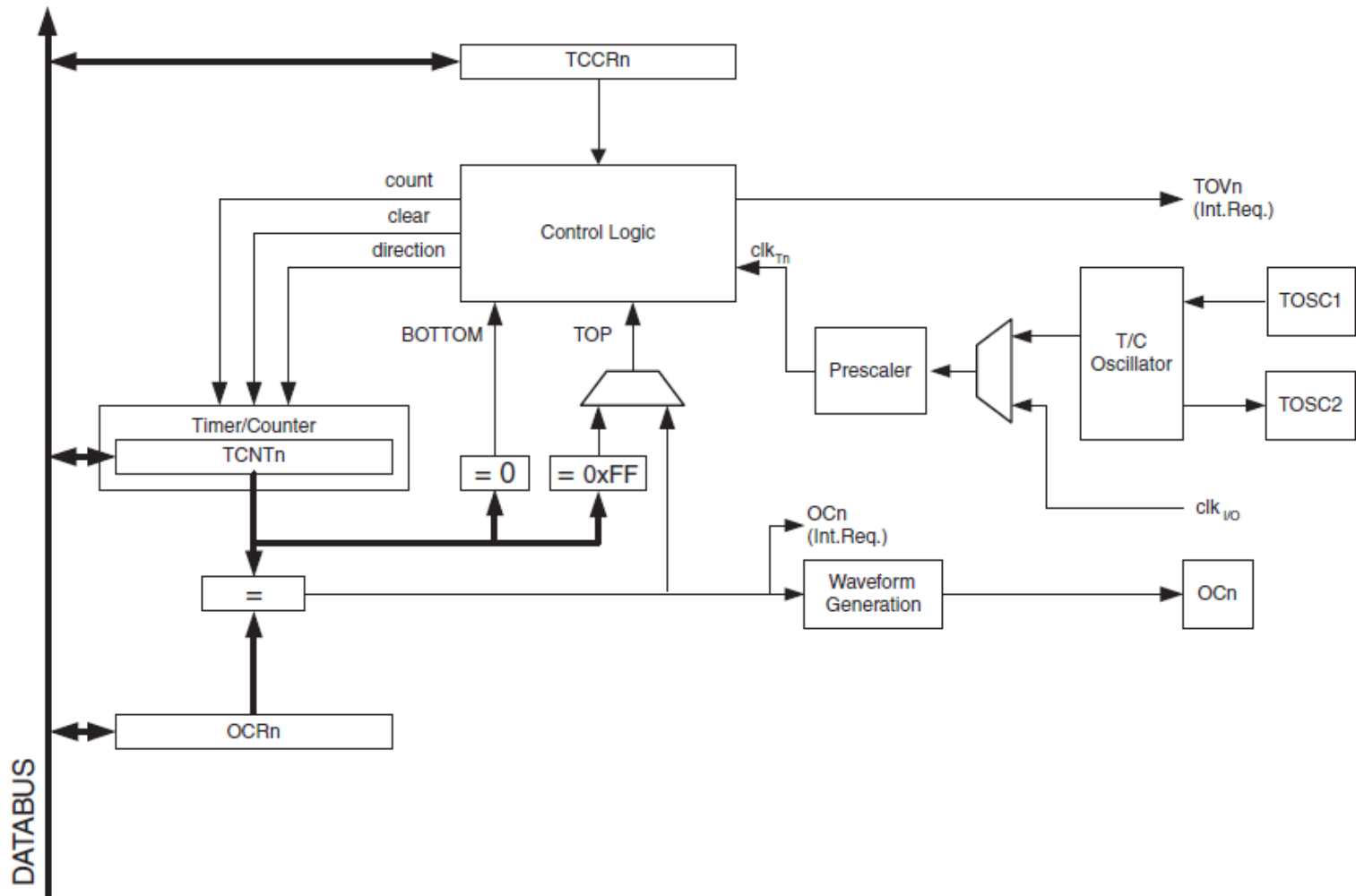
Timer/Counter



ATmega128 Timer/Counter

| Timer/Counter | Number of Bits | Timer | Counter | Compare | Capture | Waveform |
|---------------|----------------|-------|---------|---------|---------|----------|
| 0 | 8 | O | X | O | X | O |
| 1 | 16 | O | O | O | O | O |
| 2 | 8 | O | O | O | X | O |
| 3 | 16 | O | O | O | O | O |

8-bit Timer/Counter Block Diagram



Definitions

Table 51. Definitions

| | |
|--------|--|
| BOTTOM | The counter reaches the BOTTOM when it becomes zero (0x00). |
| MAX | The counter reaches its MAXimum when it becomes 0xFF (decimal 255). |
| TOP | The counter reaches the TOP when it becomes equal to the highest value in the count sequence. The TOP value can be assigned to be the fixed value 0xFF (MAX) or the value stored in the OCR0 Register. The assignment is dependent on the mode of operation. |

Clock Sources

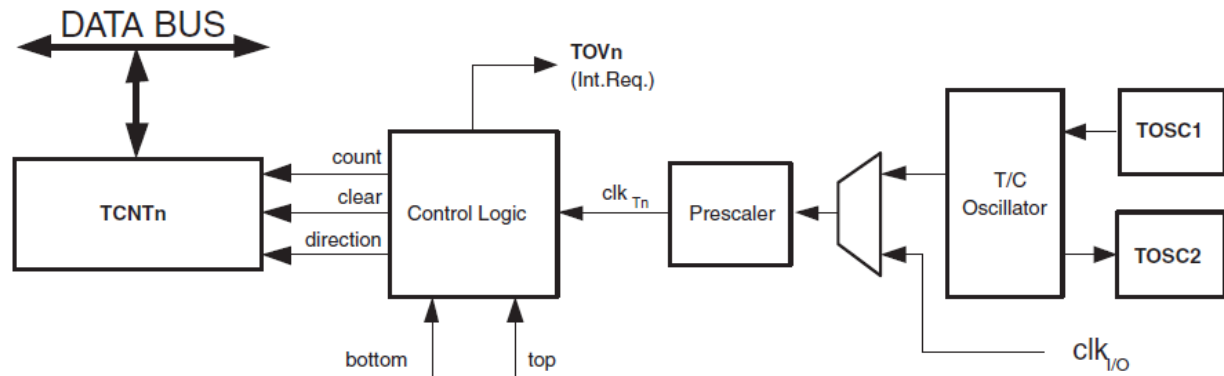
Timer/Counter Clock Sources

The Timer/Counter can be clocked by an internal synchronous or an external asynchronous clock source. The clock source clk_{T0} is by default equal to the MCU clock, $clk_{I/O}$. When the AS0 bit in the ASSR Register is written to logic one, the clock source is taken from the Timer/Counter Oscillator connected to TOSC1 and TOSC2. For details on asynchronous operation, see [“Asynchronous Status Register – ASSR” on page 107](#). For details on clock sources and prescaler, see [“Timer/Counter Prescaler” on page 110](#).

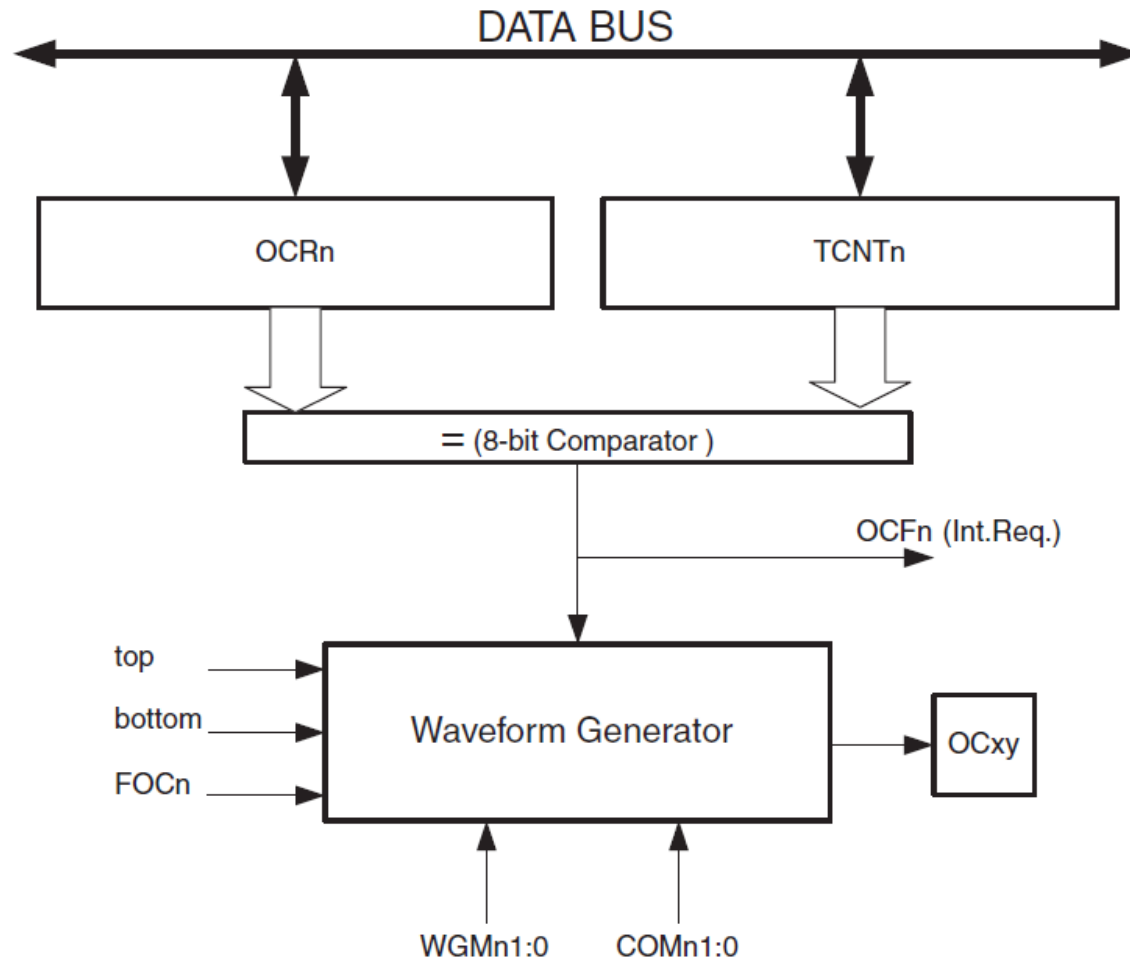
Counter Unit

The main part of the 8-bit Timer/Counter is the programmable bi-directional counter unit. [Figure 35](#) shows a block diagram of the counter and its surrounding environment.

Figure 35. Counter Unit Block Diagram



Output Compare Unit



Modes of Operation

- Normal Mode
- Clear Timer on Compare Match(CTC) Mode
- Fast PWM Mode
- Phase Correct PWM Mode

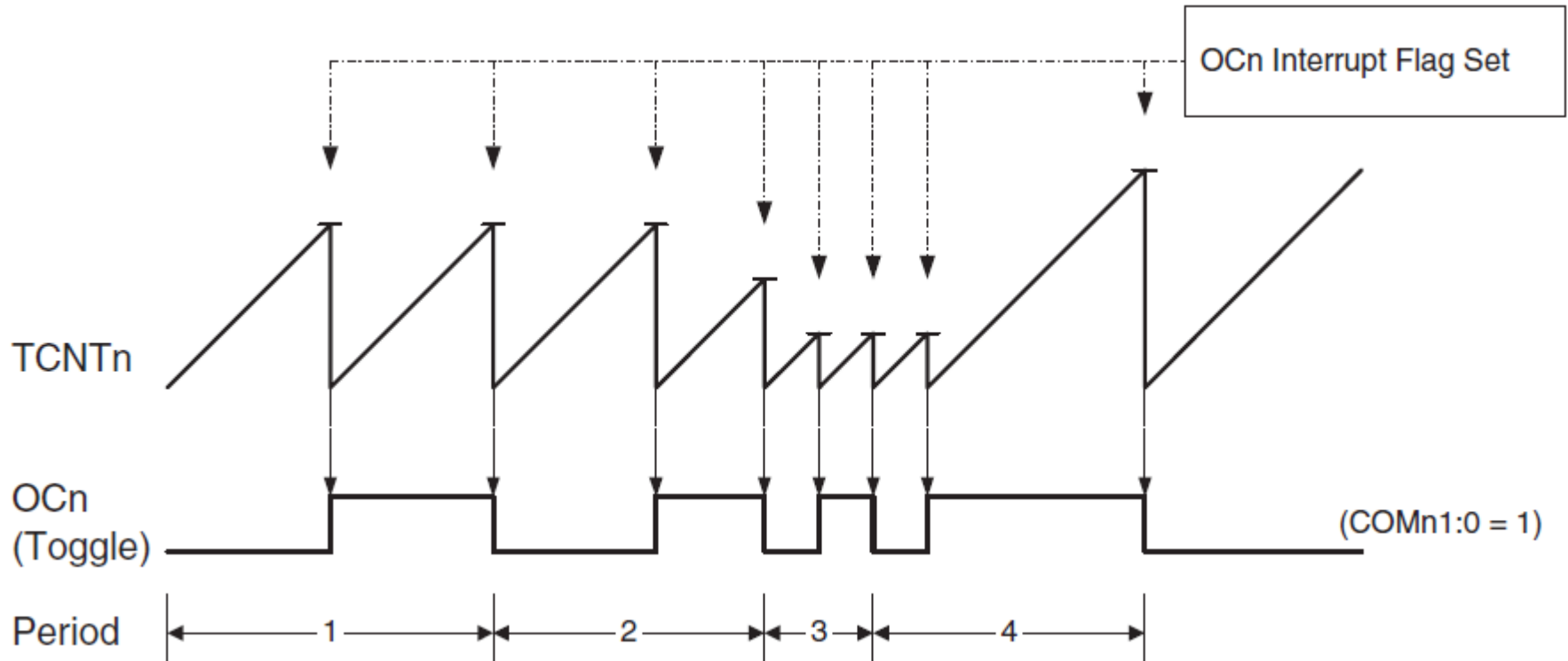
Normal Mode

- The simplest mode of operation is the normal mode ($WGM01:0 = 0$).
- In this mode the counting direction is always up (incrementing), and no counter clear is performed. The counter simply overruns when it passes its maximum 8-bit value ($TOP = 0xFF$) and then restarts from the bottom ($0x00$).
- In normal operation the Timer/Counter overflow flag ($TOV0$) will be set in the same timer clock cycle as the $TCNT0$ becomes zero.

CTC Mode

- In Clear Timer on Compare or CTC mode ($WGM01:0 = 2$), the OCR0 Register is used to manipulate the counter resolution.
- In CTC mode the counter is cleared to zero when the counter value (TCNT0) matches the OCR0. The OCR0 defines the top value for the counter, hence also its resolution.
- An interrupt can be generated each time the counter value reaches the TOP value by using the OCF0 flag. If the interrupt is enabled, the interrupt handler routine can be used for updating the TOP value.

CTC Mode



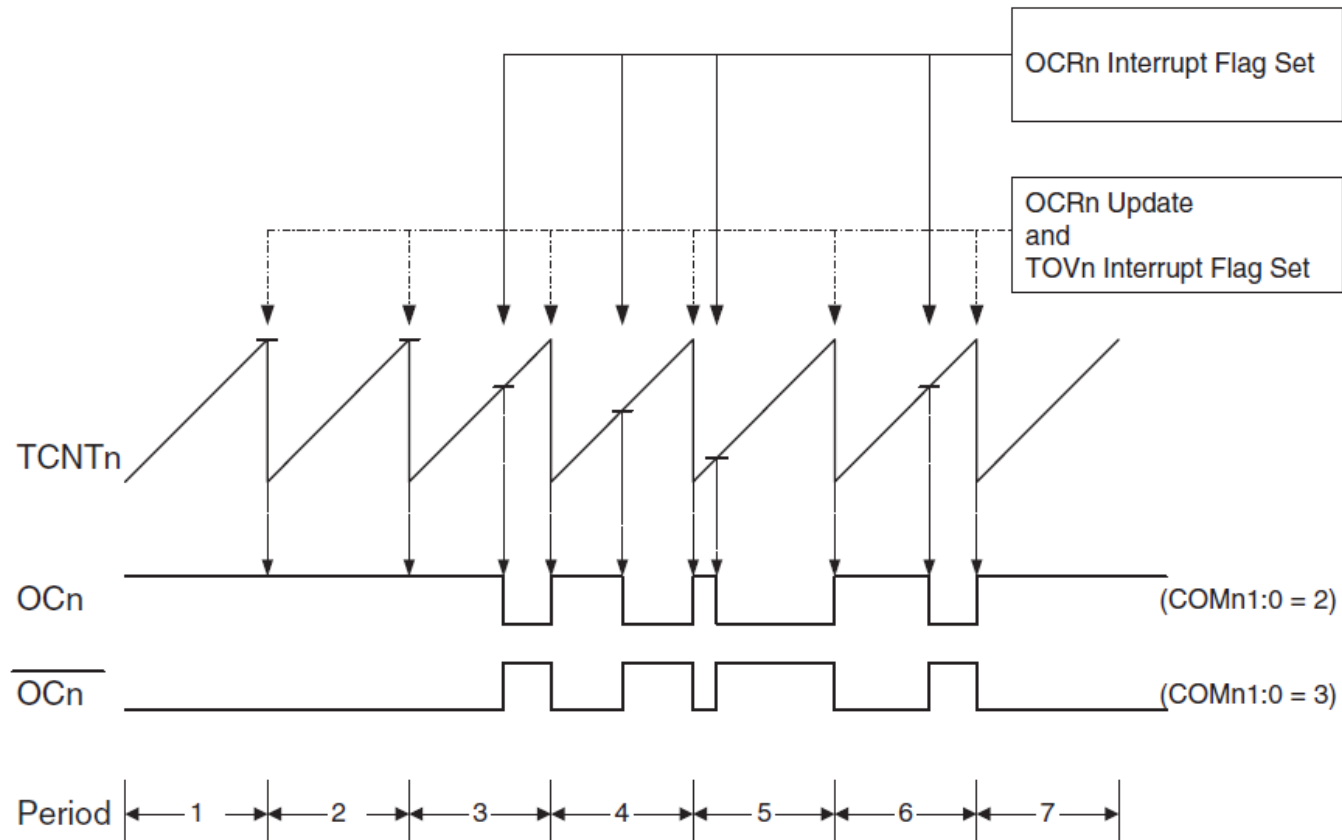
$$f_{OCn} = \frac{f_{clk_I/O}}{2 \cdot N \cdot (1 + OCRn)}$$

The N variable represents the prescale factor (1, 8, 32, 64, 128, 256, or 1024).

Fast PWM Mode

- The fast Pulse Width Modulation or fast PWM mode (WGM01:0 = 3) provides a high frequency PWM waveform generation option.
- The fast PWM differs from the other PWM option by its single-slope operation. The counter counts from BOTTOM to MAX then restarts from BOTTOM.
- In non-inverting Compare Output mode, the output compare (OC0) is cleared on the compare match between TCNT0 and OCR0, and set at BOTTOM.
- In inverting Compare Output mode, the output is set on compare match and cleared at BOTTOM. Due to the single-slope operation, the operating frequency of the fast PWM mode can be twice as high as the phase correct PWM mode that uses dual-slope operation.

Fast PWM Mode



The PWM frequency for the output can be calculated by the following equation:

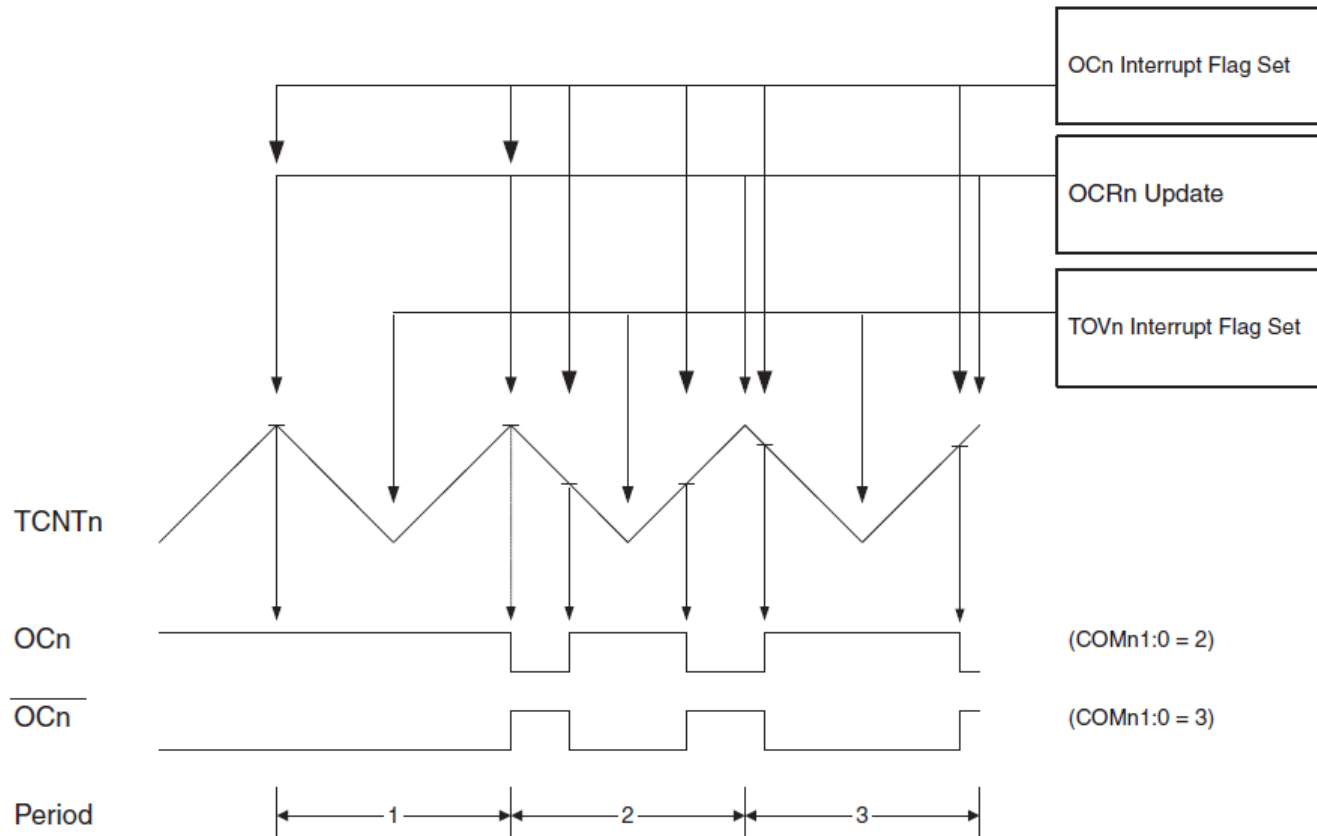
$$f_{OCnPWM} = \frac{f_{clk_I/O}}{N \cdot 256}$$

The N variable represents the prescale factor (1, 8, 32, 64, 128, 256, or 1024).

Phase Correct PWM Mode

- The phase correct PWM mode ($WGM01:0 = 1$) provides a high resolution phase correct PWM waveform generation option.
- The phase correct PWM mode is based on a dual-slope operation. The counter counts repeatedly from BOTTOM to MAX and then from MAX to BOTTOM.
- In noninverting Compare Output mode, the output compare (OC0) is cleared on the compare match between TCNT0 and OCR0 while counting up, and set on the compare match while down counting.
- In inverting Output Compare mode, the operation is inverted. The dual-slope operation has lower maximum operation frequency than single slope operation.

Phase Correct PWM Mode



PWM frequency for the output when using phase correct PWM can be calculated by the following equation:

$$f_{OCnPCPWM} = \frac{f_{clk_I/O}}{N \cdot 510}$$

The N variable represents the prescale factor (1, 8, 32, 64, 128, 256, or 1024).

TCCR0

Timer/Counter Control Register – TCCR0

| | | | | | | | | | |
|---------------|-------------|--------------|--------------|--------------|--------------|-------------|-------------|-------------|-------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | FOC0 | WGM00 | COM01 | COM00 | WGM01 | CS02 | CS01 | CS00 | TCCR0 |
| Read/Write | W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

- **Bit 6, 3 – WGM01:0: Waveform Generation Mode**

These bits control the counting sequence of the counter, the source for the maximum (TOP) counter value, and what type of waveform generation to be used. Modes of operation supported by the Timer/Counter unit are: Normal mode, Clear Timer on Compare match (CTC) mode, and two types of Pulse Width Modulation (PWM) modes. See [Table 52](#) and “Modes of Operation” on [page 98](#).

Table 52. Waveform Generation Mode Bit Description

| Mode | WGM01 ⁽¹⁾ (CTC0) | WGM00 ⁽¹⁾ (PWM0) | Timer/Counter Mode of Operation | TOP | Update of OCR0 at | TOV0 Flag Set on |
|------|--------------------------------|--------------------------------|------------------------------------|------|----------------------|---------------------|
| 0 | 0 | 0 | Normal | 0xFF | Immediate | MAX |
| 1 | 0 | 1 | PWM, Phase Correct | 0xFF | TOP | BOTTOM |
| 2 | 1 | 0 | CTC | OCR0 | Immediate | MAX |
| 3 | 1 | 1 | Fast PWM | 0xFF | BOTTOM | MAX |

- **Bit 5:4 – COM01:0: Compare Match Output Mode**

These bits control the output compare pin (OC0) behavior. If one or both of the COM01:0 bits are set, the OC0 output overrides the normal port functionality of the I/O pin it is connected to. However, note that the Data Direction Register (DDR) bit corresponding to OC0 pin must be set in order to enable the output driver.

Table 53. Compare Output Mode, non-PWM Mode

| COM01 | COM00 | Description |
|-------|-------|--|
| 0 | 0 | Normal port operation, OC0 disconnected. |
| 0 | 1 | Toggle OC0 on compare match |
| 1 | 0 | Clear OC0 on compare match |
| 1 | 1 | Set OC0 on compare match |

Table 54. Compare Output Mode, Fast PWM Mode⁽¹⁾

| COM01 | COM00 | Description |
|-------|-------|---|
| 0 | 0 | Normal port operation, OC0 disconnected. |
| 0 | 1 | Reserved |
| 1 | 0 | Clear OC0 on compare match, set OC0 at BOTTOM, (non-inverting mode) |
| 1 | 1 | Set OC0 on compare match, clear OC0 at BOTTOM, (inverting mode) |

Table 55. Compare Output Mode, Phase Correct PWM Mode⁽¹⁾

| COM01 | COM00 | Description |
|-------|-------|--|
| 0 | 0 | Normal port operation, OC0 disconnected. |
| 0 | 1 | Reserved |
| 1 | 0 | Clear OC0 on compare match when up-counting. Set OC0 on compare match when downcounting. |
| 1 | 1 | Set OC0 on compare match when up-counting. Clear OC0 on compare match when downcounting. |

TCCR0

- **Bit 2:0 – CS02:0: Clock Select**

The three clock select bits select the clock source to be used by the Timer/Counter, see [Table 56](#).

Table 56. Clock Select Bit Description

| CS02 | CS01 | CS00 | Description |
|------|------|------|---|
| 0 | 0 | 0 | No clock source (Timer/Counter stopped) |
| 0 | 0 | 1 | clk_{T0S} /(No prescaling) |
| 0 | 1 | 0 | $\text{clk}_{\text{T0S}}/8$ (From prescaler) |
| 0 | 1 | 1 | $\text{clk}_{\text{T0S}}/32$ (From prescaler) |
| 1 | 0 | 0 | $\text{clk}_{\text{T0S}}/64$ (From prescaler) |
| 1 | 0 | 1 | $\text{clk}_{\text{T0S}}/128$ (From prescaler) |
| 1 | 1 | 0 | $\text{clk}_{\text{T0S}}/256$ (From prescaler) |
| 1 | 1 | 1 | $\text{clk}_{\text{T0S}}/1024$ (From prescaler) |

TCNT0, OCR0

Timer/Counter Register – TCNT0

| | | | | | | | | | |
|---------------|------------|-----|-----|-----|-----|-----|-----|-----|-------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | TCNT0[7:0] | | | | | | | | TCNT0 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

The Timer/Counter Register gives direct access, both for read and write operations, to the Timer/Counter unit 8-bit counter. Writing to the TCNT0 Register blocks (removes) the compare match on the following timer clock. Modifying the counter (TCNT0) while the counter is running, introduces a risk of missing a compare match between TCNT0 and the OCR0 Register.

Output Compare Register – OCR0

| | | | | | | | | | |
|---------------|-----------|-----|-----|-----|-----|-----|-----|-----|------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | OCR0[7:0] | | | | | | | | OCR0 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

The Output Compare Register contains an 8-bit value that is continuously compared with the counter value (TCNT0). A match can be used to generate an output compare interrupt, or to generate a waveform output on the OC0 pin.

Timer/Counter Interrupt Mask Register – TIMSK

| | | | | | | | | | | | | | | | | | |
|---------------|--|--------|--------|--------|-------|-------|-------|-----|-------|-------|--------|--------|--------|-------|-------|-------|-------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | | | | | | |
| | <table border="1"><tr><td>OCIE2</td><td>TOIE2</td><td>TICIE1</td><td>OCIE1A</td><td>OCIE1B</td><td>TOIE1</td><td>OCIE0</td><td>TOIE0</td></tr></table> | | | | | | | | OCIE2 | TOIE2 | TICIE1 | OCIE1A | OCIE1B | TOIE1 | OCIE0 | TOIE0 | TIMSK |
| OCIE2 | TOIE2 | TICIE1 | OCIE1A | OCIE1B | TOIE1 | OCIE0 | TOIE0 | | | | | | | | | | |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | | | | | | | | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | |

- **Bit 1 – OCIE0: Timer/Counter0 Output Compare Match Interrupt Enable**

When the OCIE0 bit is written to one, and the I-bit in the Status Register is set (one), the Timer/Counter0 Compare Match interrupt is enabled. The corresponding interrupt is executed if a compare match in Timer/Counter0 occurs, i.e., when the OCF0 bit is set in the Timer/Counter Interrupt Flag Register – TIFR.

- **Bit 0 – TOIE0: Timer/Counter0 Overflow Interrupt Enable**

When the TOIE0 bit is written to one, and the I-bit in the Status Register is set (one), the Timer/Counter0 Overflow interrupt is enabled. The corresponding interrupt is executed if an overflow in Timer/Counter0 occurs, i.e., when the TOV0 bit is set in the Timer/Counter Interrupt Flag Register – TIFR.

Timer/Counter Interrupt Flag Register – TIFR

| | | | | | | | | | |
|---------------|------|------|------|-------|-------|------|------|------|------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | OCF2 | TOV2 | ICF1 | OCF1A | OCF1B | TOV1 | OCF0 | TOV0 | TIFR |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

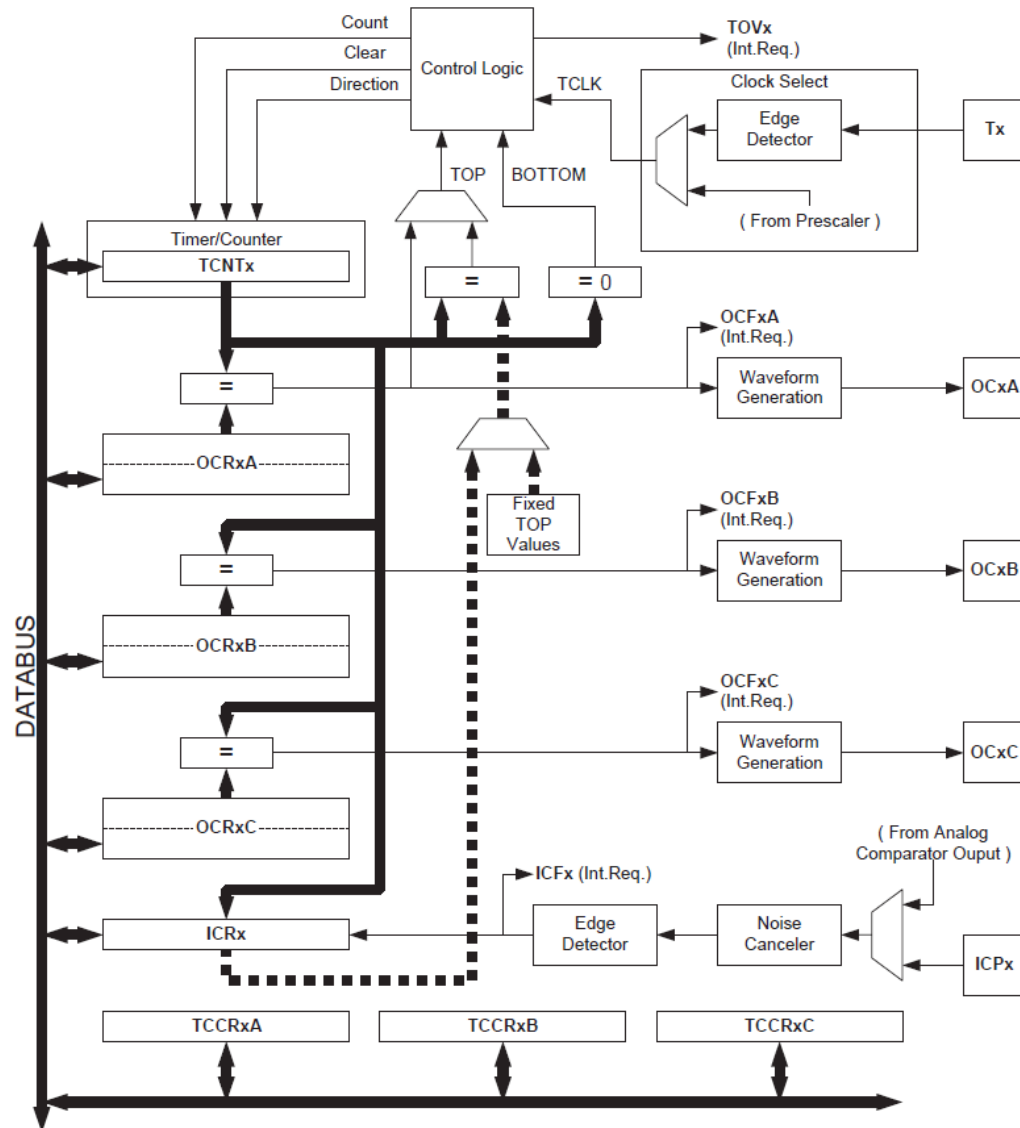
- **Bit 1 – OCF0: Output Compare Flag 0**

The OCF0 bit is set (one) when a compare match occurs between the Timer/Counter0 and the data in OCR0 – Output Compare Register0. OCF0 is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, OCF0 is cleared by writing a logic one to the flag. When the I-bit in SREG, OCIE0 (Timer/Counter0 Compare Match Interrupt Enable), and OCF0 are set (one), the Timer/Counter0 Compare Match Interrupt is executed.

- **Bit 0 – TOV0: Timer/Counter0 Overflow Flag**

The bit TOV0 is set (one) when an overflow occurs in Timer/Counter0. TOV0 is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, TOV0 is cleared by writing a logic one to the flag. When the SREG I-bit, TOIE0 (Timer/Counter0 Overflow Interrupt Enable), and TOV0 are set (one), the Timer/Counter0 Overflow Interrupt is executed. In PWM mode, this bit is set when Timer/Counter0 changes counting direction at \$00.

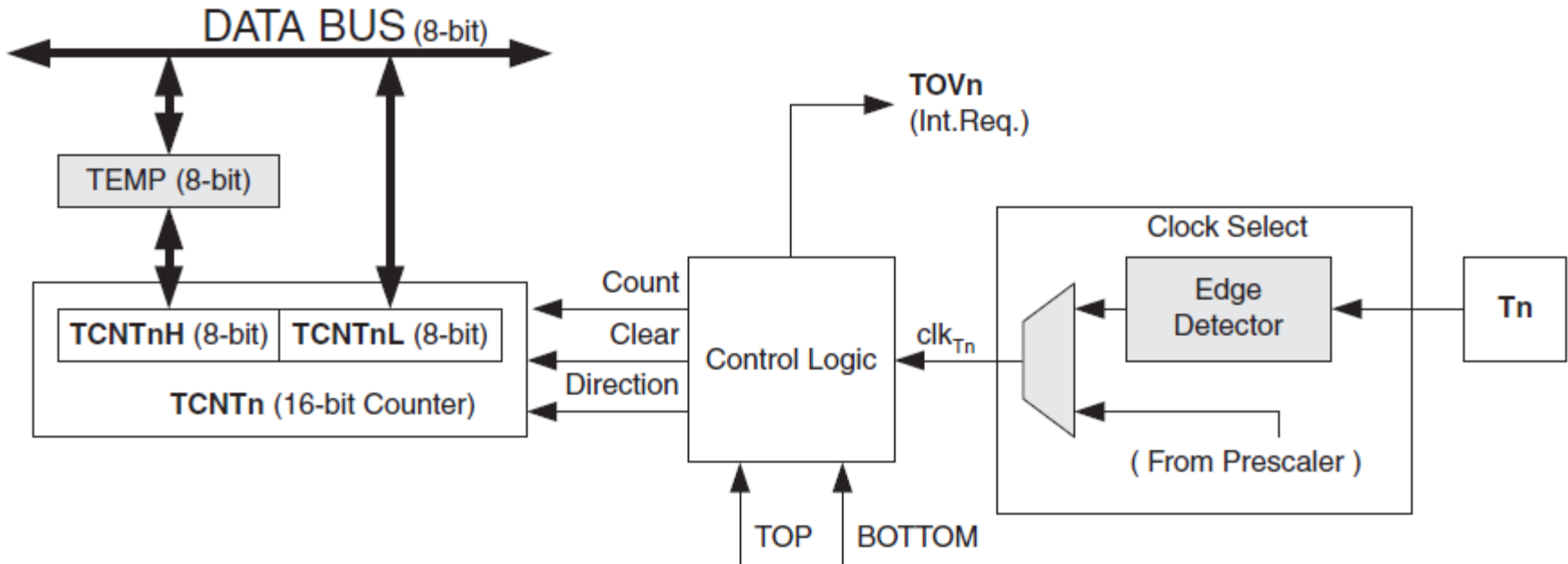
16-bit Timer/Counter Block Diagram



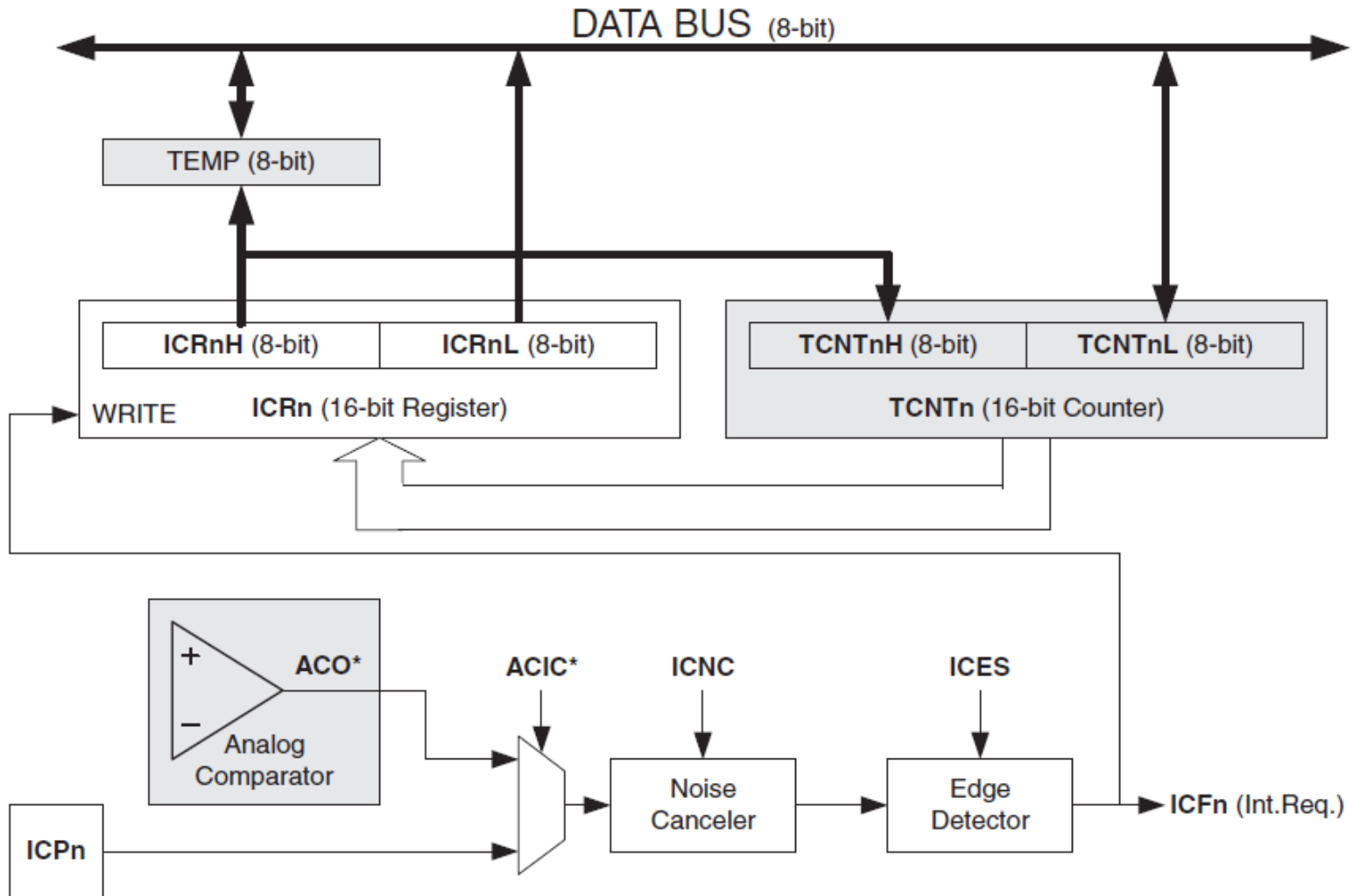
Definitions

| | |
|--------|---|
| BOTTOM | The counter reaches the <i>BOTTOM</i> when it becomes 0x0000. |
| MAX | The counter reaches its <i>MAX</i> imum when it becomes 0xFFFF (decimal 65535). |
| TOP | The counter reaches the <i>TOP</i> when it becomes equal to the highest value in the count sequence. The <i>TOP</i> value can be assigned to be one of the fixed values: 0x00FF, 0x01FF, or 0x03FF, or to the value stored in the OCRnA or ICRn Register. The assignment is dependent of the mode of operation. |

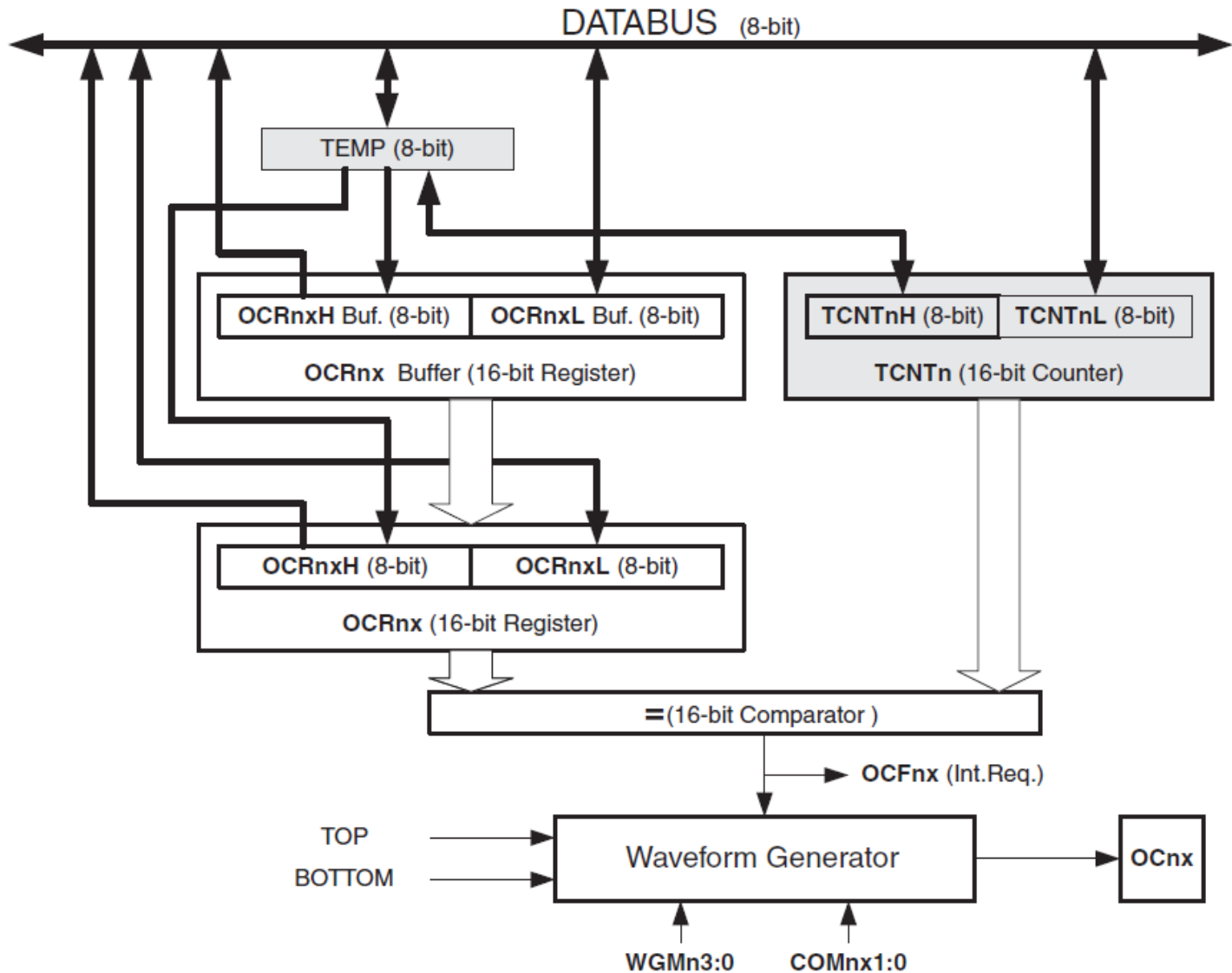
Clock Sources



Input Capture Unit



Output Compare Unit



Modes of Operation

- Normal Mode
- Clear Timer on Compare Match(CTC) Mode
- Fast PWM Mode
- Phase Correct PWM Mode
- Phase and Frequency Correct PWM Mode

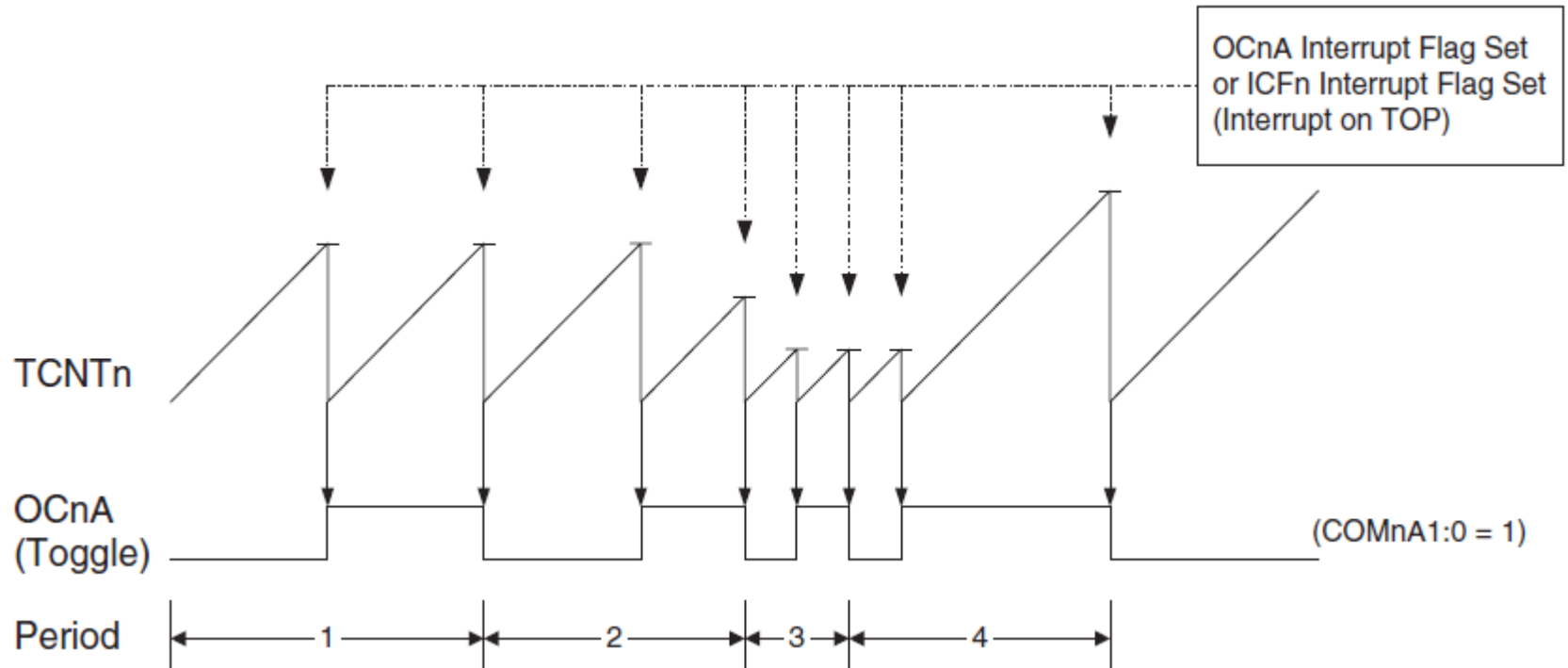
Normal Mode

- The simplest mode of operation is the normal mode ($WGMn3:0 = 0$).
- In this mode the counting direction is always up (incrementing), and no counter clear is performed. The counter simply overruns when it passes its maximum 16-bit value ($MAX = 0xFFFF$) and then restarts from the BOTTOM ($0x0000$).
- In normal operation the Timer/Counter Overflow Flag ($TOVn$) will be set in the same timer clock cycle as the $TCNTn$ becomes zero.

CTC Mode

- In Clear Timer on Compare or CTC mode ($WGMn3:0 = 4$ or 12), the $OCRnA$ or $ICRn$ Register are used to manipulate the counter resolution.
- In CTC mode the counter is cleared to zero when the counter value ($TCNTn$) matches either the $OCRnA$ ($WGMn3:0 = 4$) or the $ICRn$ ($WGMn3:0 = 12$).
- The $OCRnA$ or $ICRn$ define the top value for the counter, hence also its resolution.

CTC Mode



$$f_{OCnA} = \frac{f_{clk_I/O}}{2 \cdot N \cdot (1 + OCRnA)}$$

The N variable represents the prescaler factor (1, 8, 64, 256, or 1024).

CTC Mode

- An interrupt can be generated at each time the counter value reaches the TOP value by either using the OCFnA or ICFn flag according to the register used to define the TOP value. If the interrupt is enabled, the interrupt handler routine can be used for updating the TOP value.

Fast PWM Mode

- The fast Pulse Width Modulation or fast PWM mode (WGMn3:0 = 5,6,7,14, or 15) provides a high frequency PWM waveform generation option.
- The fast PWM differs from the other PWM options by its single-slope operation. The counter counts from BOTTOM to TOP then restarts from BOTTOM.
- In non-inverting Compare Output mode, the output compare (OCnx) is cleared on the compare match between TCNTn and OCRnx, and set at BOTTOM.
- In inverting compare output mode output is set on compare match and cleared at BOTTOM.

Fast PWM Mode

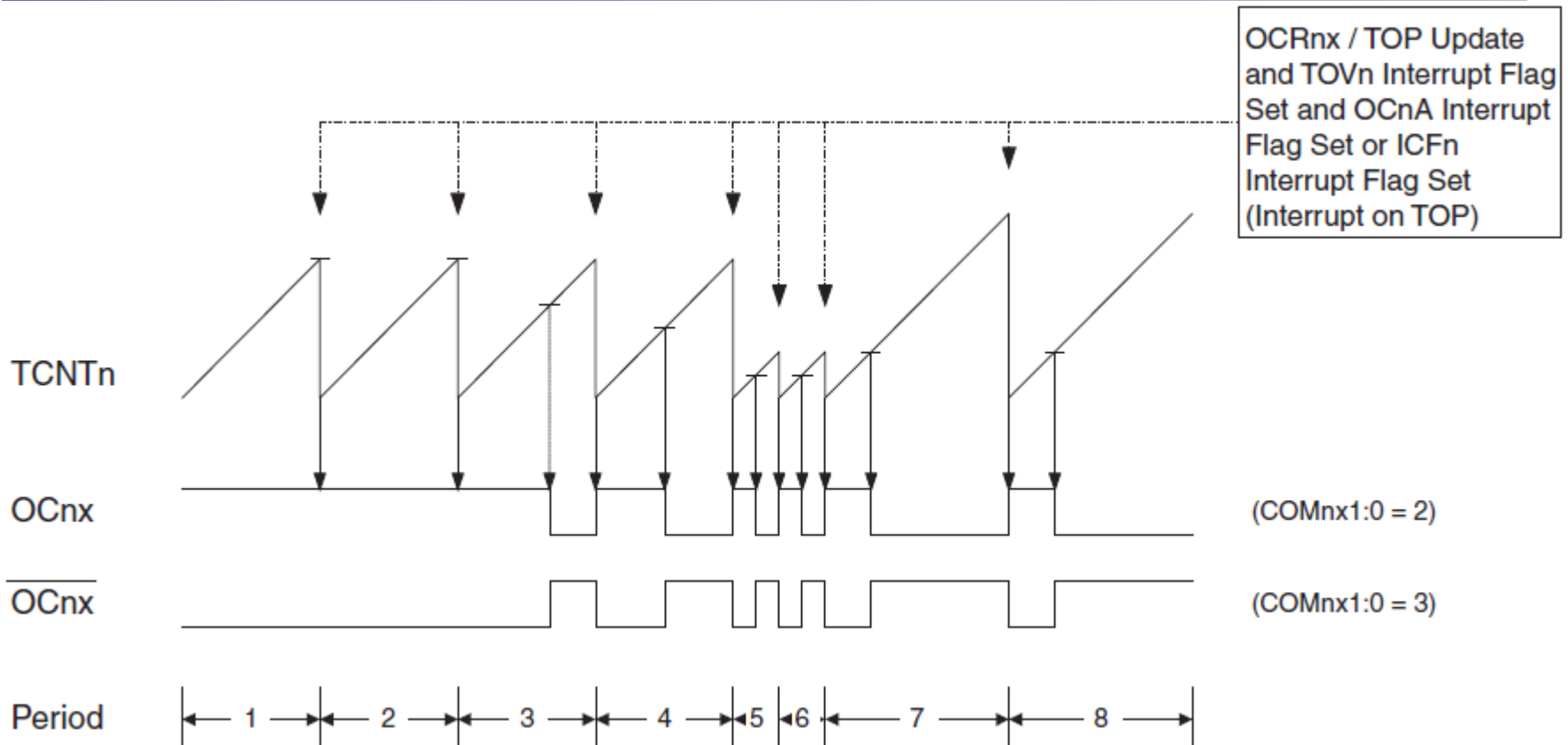
- Due to the single-slope operation, the operating frequency of the fast PWM mode can be twice as high as the phase correct and phase and frequency correct PWM modes that use dual-slope operation.
- The PWM resolution for fast PWM can be fixed to 8-, 9-, or 10-bit, or defined by either ICRn or OCRnA. The minimum resolution allowed is 2-bit (ICRn or OCRnA set to 0x0003), and the maximum resolution is 16-bit (ICRn or OCRnA set to MAX). The PWM resolution in bits can be calculated by using the following equation:

$$R_{FPWM} = \frac{\log(TOP + 1)}{\log(2)}$$

Fast PWM Mode

- In fast PWM mode the counter is incremented until the counter value matches either one of the fixed values 0x00FF, 0x01FF, or 0x03FF ($WGMn3:0 = 5, 6, \text{ or } 7$), the value in ICRn ($WGMn3:0 = 14$), or the value in OCRnA ($WGMn3:0 = 15$). The counter is then cleared at the following timer clock cycle.

Fast PWM Mode



The PWM frequency for the output can be calculated by the following equation:

$$f_{OCnxPWM} = \frac{f_{clk_I/O}}{N \cdot (1 + TOP)}$$

The N variable represents the prescaler divider (1, 8, 64, 256, or 1024).

Phase Correct PWM Mode

- The phase correct Pulse Width Modulation or phase correct PWM mode ($WGMn3:0 = 1, 2, 3, 10, \text{ or } 11$) provides a high resolution phase correct PWM waveform generation option.
- The phase correct PWM mode is, like the phase and frequency correct PWM mode, based on a dual slope operation. The counter counts repeatedly from BOTTOM (0x0000) to TOP and then from TOP to BOTTOM.
- In non-inverting compare output mode, the output compare (OCnx) is cleared on the compare match between TCNTn and OCRnx while counting up, and set on the compare match while down counting.

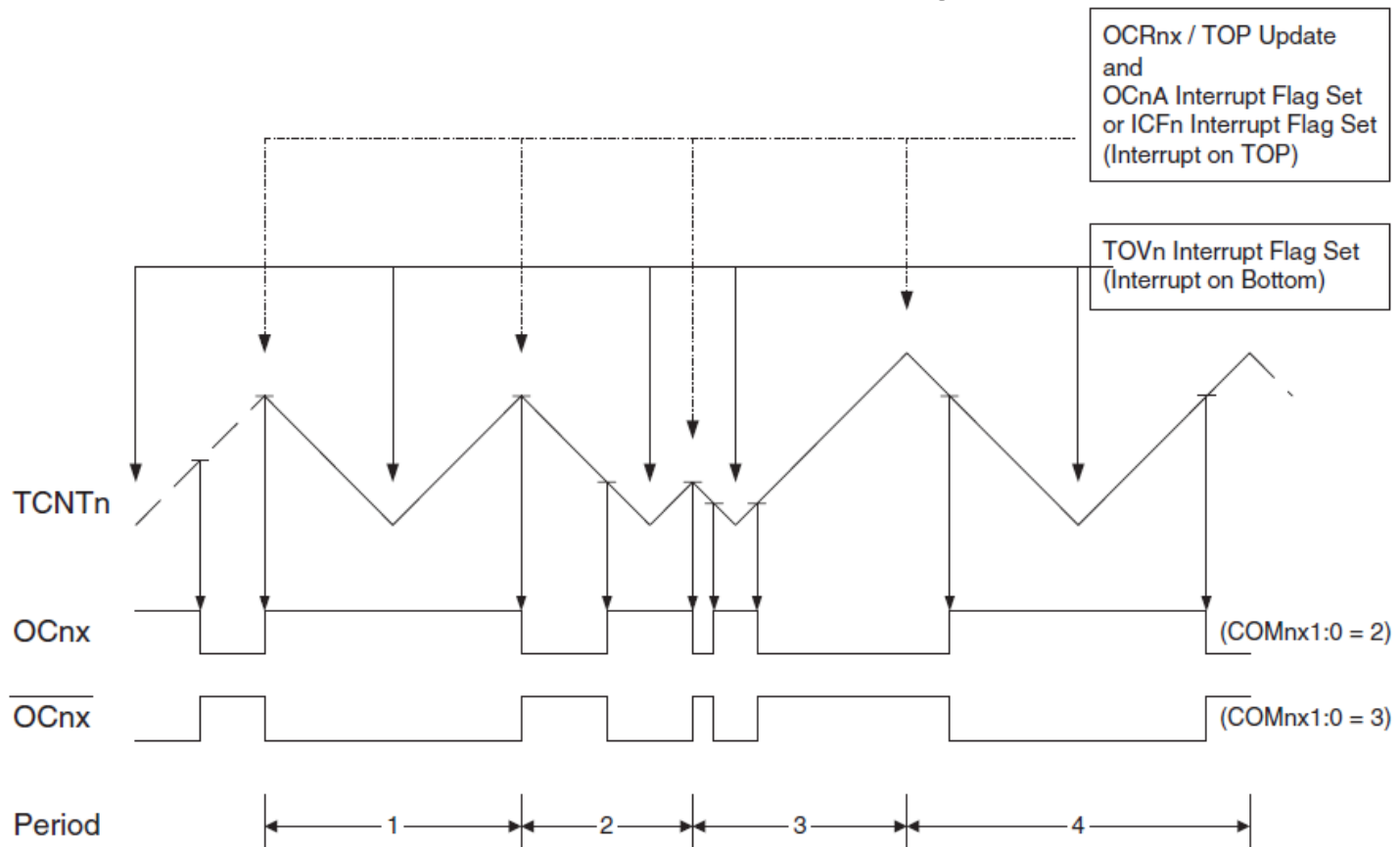
Phase Correct PWM Mode

- In inverting Output Compare mode, the operation is inverted. The dual-slope operation has lower maximum operation frequency than single slope operation. However, due to the symmetric feature of the dual-slope PWM modes, these modes are preferred for motor control applications.
- The PWM resolution for the phase correct PWM mode can be fixed to 8-, 9-, or 10-bit, or defined by either ICRn or OCRnA. The minimum resolution allowed is 2 bit (ICRn or OCRnA set to 0x0003), and the maximum resolution is 16 bit (ICRn or OCRnA set to MAX). The PWM resolution in bits can be calculated by using the following equation:

$$R_{PCPWM} = \frac{\log(TOP + 1)}{\log(2)}$$

Phase Correct PWM Mode

- In phase correct PWM mode the counter is incremented until the counter value matches either one of the fixed values 0x00FF, 0x01FF, or 0x03FF ($WGMn3:0 = 1, 2, \text{ or } 3$), the value in $ICRn$ ($WGMn3:0 = 10$), or the value in $OCRnA$ ($WGMn3:0 = 11$). The counter has then reached the TOP and changes the count direction.



Phase Correct PWM Mode

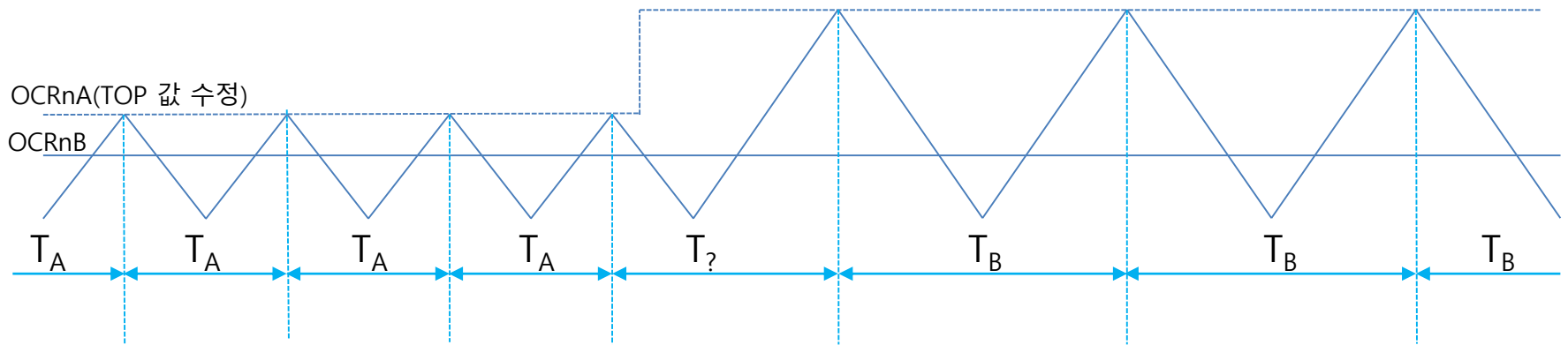
- The PWM frequency for the output when using phase correct PWM can be calculated by the following equation:

$$f_{OCnxPCPWM} = \frac{f_{clk_I/O}}{2 \cdot N \cdot TOP}$$

- The N variable represents the prescaler divider (1, 8, 64, 256, or 1024).

Phase Correct PWM Mode

- Frequency Distortion



Phase and Frequency Correct PWM Mode

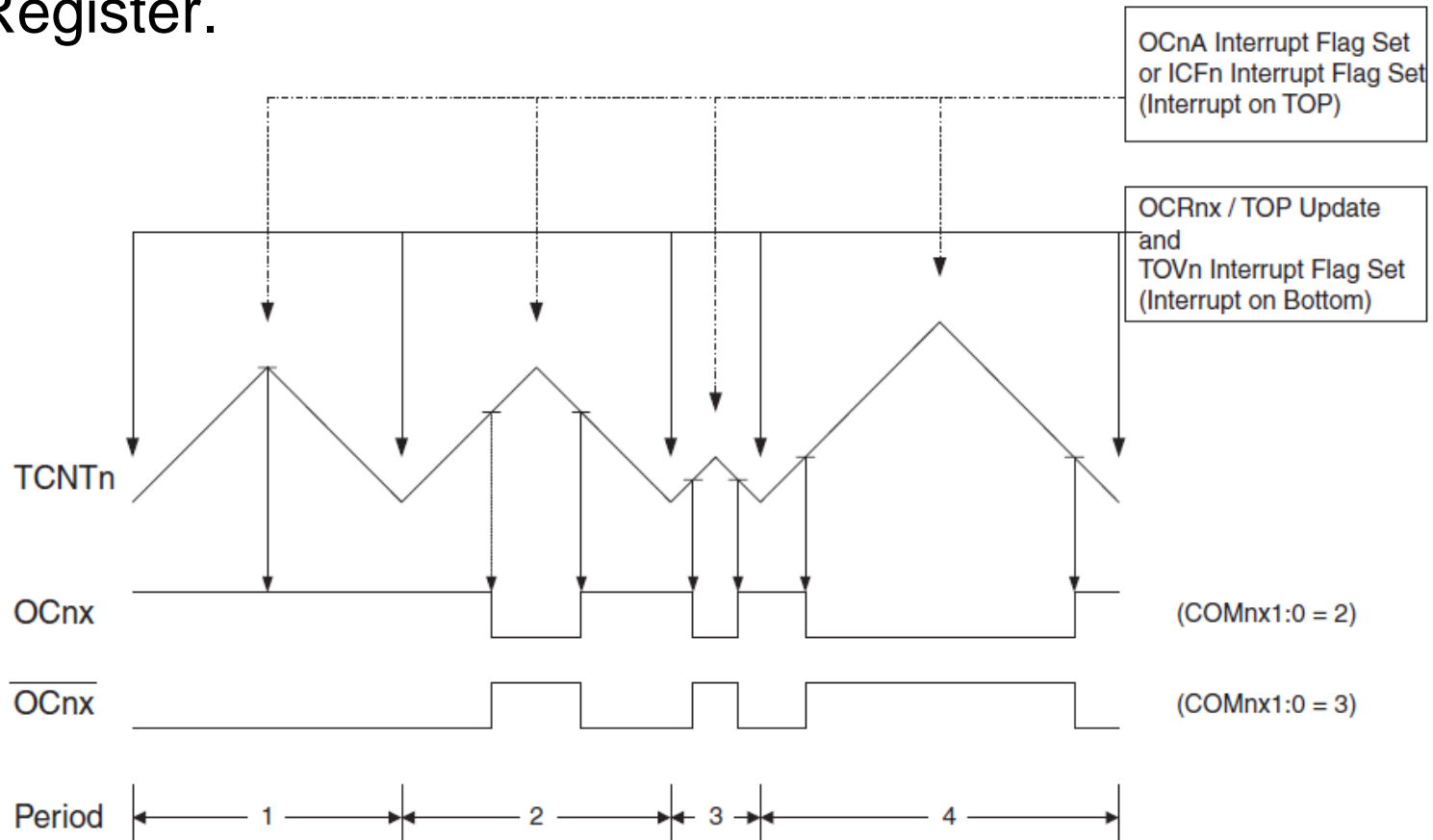
- The phase and frequency correct Pulse Width Modulation, or phase and frequency correct PWM mode (WGMn3:0 = 8 or 9) provides a high resolution phase and frequency correct PWM waveform generation option.
- The phase and frequency correct PWM mode is, like the phase correct PWM mode, based on a dual-slope operation. The counter counts repeatedly from BOTTOM (0x0000) to TOP and then from TOP to BOTTOM.

Phase and Frequency Correct PWM Mode

- In non-inverting Compare Output mode, the output compare (OCnx) is cleared on the compare match between TCNTn and OCRnx while counting up, and set on the compare match while down counting. In inverting Compare Output mode, the operation is inverted.
- The dual-slope operation gives a lower maximum operation frequency compared to the single-slope operation. However, due to the symmetric feature of the dual-slope PWM modes, these modes are preferred for motor control applications.

Phase and Frequency Correct PWM Mode

- The main difference between the phase correct, and the phase and frequency correct PWM mode is the time the OCRnx Register is updated by the OCRnx buffer Register.



Phase and Frequency Correct PWM Mode

- The PWM resolution for the phase and frequency correct PWM mode can be defined by either ICRn or OCRnA. The minimum resolution allowed is 2-bit (ICRn or OCRnA set to 0x0003), and the maximum resolution is 16-bit (ICRn or OCRnA set to MAX). The PWM resolution in bits can be calculated using the following equation:

$$R_{PFCPWM} = \frac{\log(TOP + 1)}{\log(2)}$$

- In phase and frequency correct PWM mode the counter is incremented until the counter value matches either the value in ICRn (WGMn3:0 = 8), or the value in OCRnA (WGMn3:0 = 9). The counter has then reached the TOP and changes the count direction.

Phase and Frequency Correct PWM Mode

- The PWM frequency for the output when using phase and frequency correct PWM can be calculated by the following equation:

$$f_{OCnxPCPWM} = \frac{f_{clk_I/O}}{2 \cdot N \cdot TOP}$$

- The N variable represents the prescaler divider (1, 8, 64, 256, or 1024).

16-bit Timer/Counter1,3 Control Register A (TCCR1A, TCCR3A)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---------------|--------|--------|--------|--------|--------|--------|-------|-------|--------|
| | COM1A1 | COM1A0 | COM1B1 | COM1B0 | COM1C1 | COM1C0 | WGM11 | WGM10 | TCCR1A |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---------------|--------|--------|--------|--------|--------|--------|-------|-------|--------|
| | COM3A1 | COM3A0 | COM3B1 | COM3B0 | COM3C1 | COM3C0 | WGM31 | WGM30 | TCCR3A |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

- **Bit 7:6 – COMnA1:0: Compare Output Mode for Channel A**
- **Bit 5:4 – COMnB1:0: Compare Output Mode for Channel B**
- **Bit 3:2 – COMnC1:0: Compare Output Mode for Channel C**

The COMnA1:0, COMnB1:0, and COMnC1:0 control the output compare pins (OCnA, OCnB, and OCnC respectively) behavior. If one or both of the COMnA1:0 bits are written to one, the OCnA output overrides the normal port functionality of the I/O pin it is connected to. If one or both of the COMnB1:0 bits are written to one, the OCnB output overrides the normal port functionality of the I/O pin it is connected to. If one or both of the COMnC1:0 bits are written to one, the OCnC output overrides the normal port functionality of the I/O pin it is connected to. However, note that the *Data Direction Register* (DDR) bit corresponding to the OCnA, OCnB or OCnC pin must be set in order to enable the output driver.

16-bit Timer/Counter1,3 Control Register A (TCCR1A, TCCR3A)

Table 58. Compare Output Mode, non-PWM

| COMnA1/COMnB1/ COMnC1 | COMnA0/COMnB0/ COMnC0 | Description |
|--------------------------|--------------------------|--|
| 0 | 0 | Normal port operation, OCnA/OCnB/OCnC disconnected. |
| 0 | 1 | Toggle OCnA/OCnB/OCnC on compare match. |
| 1 | 0 | Clear OCnA/OCnB/OCnC on compare match (set output to low level). |
| 1 | 1 | Set OCnA/OCnB/OCnC on compare match (set output to high level). |

16-bit Timer/Counter1,3 Control Register A (TCCR1A, TCCR3A)

Table 59. Compare Output Mode, Fast PWM

| COMnA1/COMnB1/ COMnC1 | COMnA0/COMnB0/ COMnC0 | Description |
|--------------------------|--------------------------|---|
| 0 | 0 | Normal port operation, OCnA/OCnB/OCnC disconnected. |
| 0 | 1 | WGMn3:0 = 15: Toggle OCnA on Compare Match, OCnB/OCnC disconnected (normal port operation). For all other WGMn settings, normal port operation, OCnA/OCnB/OCnC disconnected. |
| 1 | 0 | Clear OCnA/OCnB/OCnC on compare match, set OCnA/OCnB/OCnC at BOTTOM, (non-inverting mode) |
| 1 | 1 | Set OCnA/OCnB/OCnC on compare match, clear OCnA/OCnB/OCnC at BOTTOM, (inverting mode) |

16-bit Timer/Counter1,3 Control Register A (TCCR1A, TCCR3A)

Table 60. Compare Output Mode, Phase Correct and Phase and Frequency Correct PWM

| COMnA1/COMnB1/ COMnC1 | COMnA0/COMnB0/ COMnC0 | Description |
|--------------------------|--------------------------|--|
| 0 | 0 | Normal port operation, OCnA/OCnB/OCnC disconnected. |
| 0 | 1 | WGMn3:0 = 9 or 11: Toggle OCnA on Compare Match, OCnB/OCnC disconnected (normal port operation). For all other WGMn settings, normal port operation, OCnA/OCnB/OCnC disconnected. |
| 1 | 0 | Clear OCnA/OCnB/OCnC on compare match when up-counting. Set OCnA/OCnB/OCnC on compare match when downcounting. |
| 1 | 1 | Set OCnA/OCnB/OCnC on compare match when up-counting. Clear OCnA/OCnB/OCnC on compare match when downcounting. |

Timer/Counter1,3

Control Register A (TCCR1A, TCCR3A)

Table 61. Waveform Generation Mode Bit Description

| Mode | WGMn3 | WGMn2 (CTCn) | WGMn1 (PWMn1) | WGMn0 (PWMn0) | Timer/Counter Mode of Operation ⁽¹⁾ | TOP | Update of OCRnX at | TOVn Flag Set on |
|------|-------|--------------|---------------|---------------|--|--------|--------------------|------------------|
| 0 | 0 | 0 | 0 | 0 | Normal | 0xFFFF | Immediate | MAX |
| 1 | 0 | 0 | 0 | 1 | PWM, Phase Correct, 8-bit | 0x00FF | TOP | BOTTOM |
| 2 | 0 | 0 | 1 | 0 | PWM, Phase Correct, 9-bit | 0x01FF | TOP | BOTTOM |
| 3 | 0 | 0 | 1 | 1 | PWM, Phase Correct, 10-bit | 0x03FF | TOP | BOTTOM |
| 4 | 0 | 1 | 0 | 0 | CTC | OCRnA | Immediate | MAX |
| 5 | 0 | 1 | 0 | 1 | Fast PWM, 8-bit | 0x00FF | BOTTOM | TOP |
| 6 | 0 | 1 | 1 | 0 | Fast PWM, 9-bit | 0x01FF | BOTTOM | TOP |
| 7 | 0 | 1 | 1 | 1 | Fast PWM, 10-bit | 0x03FF | BOTTOM | TOP |
| 8 | 1 | 0 | 0 | 0 | PWM, Phase and Frequency Correct | ICRn | BOTTOM | BOTTOM |
| 9 | 1 | 0 | 0 | 1 | PWM, Phase and Frequency Correct | OCRnA | BOTTOM | BOTTOM |
| 10 | 1 | 0 | 1 | 0 | PWM, Phase Correct | ICRn | TOP | BOTTOM |
| 11 | 1 | 0 | 1 | 1 | PWM, Phase Correct | OCRnA | TOP | BOTTOM |
| 12 | 1 | 1 | 0 | 0 | CTC | ICRn | Immediate | MAX |
| 13 | 1 | 1 | 0 | 1 | (Reserved) | – | – | – |
| 14 | 1 | 1 | 1 | 0 | Fast PWM | ICRn | BOTTOM | TOP |
| 15 | 1 | 1 | 1 | 1 | Fast PWM | OCRnA | BOTTOM | TOP |

Note: 1. The CTCn and PWMn1:0 bit definition names are obsolete. Use the WGMn2:0 definitions. However, the functionality and location of these bits are compatible with previous versions of the timer.

Timer/Counter1,3 Control Register B (TCCR1B, TCCR3B)

Timer/Counter1 Control Register B – TCCR1B

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---------------|-------|-------|---|-------|-------|------|------|------|--------|
| | ICNC1 | ICES1 | – | WGM13 | WGM12 | CS12 | CS11 | CS10 | TCCR1B |
| Read/Write | R/W | R/W | R | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Timer/Counter3 Control Register B – TCCR3B

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---------------|-------|-------|---|-------|-------|------|------|------|--------|
| | ICNC3 | ICES3 | – | WGM33 | WGM32 | CS32 | CS31 | CS30 | TCCR3B |
| Read/Write | R/W | R/W | R | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

- **Bit 7 – ICNCn: Input Capture Noise Canceler**

Setting this bit (to one) activates the Input Capture Noise Canceler. When the Noise Canceler is activated, the input from the Input Capture Pin (ICPn) is filtered. The filter function requires four successive equal valued samples of the ICPn pin for changing its output. The Input Capture is therefore delayed by four Oscillator cycles when the noise canceler is enabled.

- **Bit 6 – ICESn: Input Capture Edge Select**

This bit selects which edge on the Input Capture Pin (ICPn) that is used to trigger a capture event. When the ICESn bit is written to zero, a falling (negative) edge is used as trigger, and when the ICESn bit is written to one, a rising (positive) edge will trigger the capture.

When a capture is triggered according to the ICESn setting, the counter value is copied into the Input Capture Register (ICRn). The event will also set the Input Capture Flag (ICFn), and this can be used to cause an Input Capture Interrupt, if this interrupt is enabled.

When the ICRn is used as TOP value (see description of the WGMn3:0 bits located in the TCCRnA and the TCCRnB Register), the ICPn is disconnected and consequently the Input Capture function is disabled.

- **Bit 5 – Reserved Bit**

This bit is reserved for future use. For ensuring compatibility with future devices, this bit must be written to zero when TCCRnB is written.

- **Bit 4:3 – WGMn3:2: Waveform Generation Mode**

See TCCRnA Register description.

- **Bit 2:0 – CSn2:0: Clock Select**

Timer/Counter1,3

Control Register B (TCCR1B, TCCR3B)

Table 62. Clock Select Bit Description

| CSn2 | CSn1 | CSn0 | Description |
|------|------|------|--|
| 0 | 0 | 0 | No clock source. (Timer/Counter stopped) |
| 0 | 0 | 1 | $clk_{IO}/1$ (No prescaling) |
| 0 | 1 | 0 | $clk_{IO}/8$ (From prescaler) |
| 0 | 1 | 1 | $clk_{IO}/64$ (From prescaler) |
| 1 | 0 | 0 | $clk_{IO}/256$ (From prescaler) |
| 1 | 0 | 1 | $clk_{IO}/1024$ (From prescaler) |
| 1 | 1 | 0 | External clock source on Tn pin. Clock on falling edge |
| 1 | 1 | 1 | External clock source on Tn pin. Clock on rising edge |

Timer/Counter Interrupt Mask Register (TIMSK)

Timer/Counter Interrupt Mask Register – TIMSK

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---------------|-------|-------|--------|--------|--------|-------|-------|-------|-------|
| | OCIE2 | TOIE2 | TICIE1 | OCIE1A | OCIE1B | TOIE1 | OCIE0 | TOIE0 | TIMSK |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Note: This register contains interrupt control bits for several Timer/Counters, but only Timer1 bits are described in this section. The remaining bits are described in their respective timer sections.

- **Bit 5 – TICIE1: Timer/Counter1, Input Capture Interrupt Enable**

When this bit is written to one, and the I-flag in the Status Register is set (interrupts globally enabled), the Timer/Counter1 Input Capture interrupt is enabled. The corresponding interrupt vector (See “Interrupts” on page 60.) is executed when the ICF1 flag, located in TIFR, is set.

- **Bit 4 – OCIE1A: Timer/Counter1, Output Compare A Match Interrupt Enable**

When this bit is written to one, and the I-flag in the Status Register is set (interrupts globally enabled), the Timer/Counter1 Output Compare A Match Interrupt is enabled. The corresponding interrupt vector (see “Interrupts” on page 60) is executed when the OCF1A flag, located in TIFR, is set.

- **Bit 3 – OCIE1B: Timer/Counter1, Output Compare B Match Interrupt Enable**

When this bit is written to one, and the I-flag in the Status Register is set (interrupts globally enabled), the Timer/Counter1 Output Compare B Match Interrupt is enabled. The corresponding interrupt vector (see “Interrupts” on page 60) is executed when the OCF1B flag, located in TIFR, is set.

- **Bit 2 – TOIE1: Timer/Counter1, Overflow Interrupt Enable**

When this bit is written to one, and the I-flag in the Status Register is set (interrupts globally enabled), the Timer/Counter1 overflow interrupt is enabled. The corresponding interrupt vector (see “Interrupts” on page 60) is executed when the TOV1 flag, located in TIFR, is set.

Extended Timer/Counter Interrupt Mask Register (ETIMSK)

Extended Timer/Counter Interrupt Mask Register – ETIMSK

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---------------|---|---|--------|--------|--------|-------|--------|--------|--------|
| | – | – | TICIE3 | OCIE3A | OCIE3B | TOIE3 | OCIE3C | OCIE1C | ETIMSK |
| Read/Write | R | R | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Note: This register is not available in ATmega103 compatibility mode.

- **Bit 7:6 – Reserved Bits**

These bits are reserved for future use. For ensuring compatibility with future devices, these bits must be set to zero when ETIMSK is written.

- **Bit 5 – TICIE3: Timer/Counter3, Input Capture Interrupt Enable**

When this bit is written to one, and the I-flag in the Status Register is set (interrupts globally enabled), the Timer/Counter3 Input Capture Interrupt is enabled. The corresponding interrupt vector (see “Interrupts” on page 60) is executed when the ICF3 flag, located in ETIFR, is set.

- **Bit 4 – OCIE3A: Timer/Counter3, Output Compare A Match Interrupt Enable**

When this bit is written to one, and the I-flag in the Status Register is set (interrupts globally enabled), the Timer/Counter3 Output Compare A Match Interrupt is enabled. The corresponding interrupt vector (see “Interrupts” on page 60) is executed when the OCF3A flag, located in ETIFR, is set.

- **Bit 3 – OCIE3B: Timer/Counter3, Output Compare B Match Interrupt Enable**

When this bit is written to one, and the I-flag in the Status Register is set (interrupts globally enabled), the Timer/Counter3 Output Compare B Match Interrupt is enabled. The corresponding interrupt vector (see “Interrupts” on page 60) is executed when the OCF3B flag, located in ETIFR, is set.

- **Bit 2 – TOIE3: Timer/Counter3, Overflow Interrupt Enable**

When this bit is written to one, and the I-flag in the Status Register is set (interrupts globally enabled), the Timer/Counter3 Overflow Interrupt is enabled. The corresponding interrupt vector (see “Interrupts” on page 60) is executed when the TOV3 flag, located in ETIFR, is set.

- **Bit 1 – OCIE3C: Timer/Counter3, Output Compare C Match Interrupt Enable**

Extended Timer/Counter Interrupt Mask Register (ETIMSK)

When this bit is written to one, and the I-flag in the Status Register is set (interrupts globally enabled), the Timer/Counter3 Output Compare C Match Interrupt is enabled. The corresponding interrupt vector (see “Interrupts” on page 60) is executed when the OCF3C flag, located in ETIFR, is set.

- **Bit 0 – OCIE1C: Timer/Counter1, Output Compare C Match Interrupt Enable**

When this bit is written to one, and the I-flag in the Status Register is set (interrupts globally enabled), the Timer/Counter1 Output Compare C Match Interrupt is enabled. The corresponding interrupt vector (see “Interrupts” on page 60) is executed when the OCF1C flag, located in ETIFR, is set.